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Development of laboratory prototype of a 12kVA digital shunt active filter

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***Abstract*-The paper reports the development of a laboratory prototype of a fully digital DSP controlled 12 kVA Shunt Active Filter (ShAF) capable of compensating for non-linear, unbalanced load and reactive power. A fully digital controller is implemented for the reference generation and the current control purposes. The delay problem in digital current controller is overcome by application of a fast DSP, a compact controller and proper flow of control steps in the DSP software. A Phase Locked Loop (PLL)-less software grid synchronization method has been proposed for the effective operation of the ShAF under the grid frequency variation. The source current THD has been improved from 15.8% to 4.45%. The control features, experimental setup, and results are presented in the paper.**

I. INTRODUCTION

The Active Filters (AF) are preferred over passive filters as solution to various Power Quality (PQ) problems arising from the load or the supply side. The few obvious reasons for this are [1]:

(1) Design of the active filters is almost independent of power system parameters.

(2) No lengthy tuning effort is required in the design of active filters, which is usual in case of passive filters

(3) Possibility of resonance is excluded in the active filter application

The various configurations of active filters are reported in [2] and [3]. The systems are inherently complex and require sophisticated control system to achieve the satisfactory performance. A fast Digital Signal Processor or a microprocessor is often utilised to carry out the complex control of the active filters. The DSP application for control of the Shunt Active Filters (ShAF) is reported in [4]-[9]. The reference current generation, and achieving the generated reference through some appropriate current control are two identified tasks under any type of control. In [4], DSP is applied to generate reference source current based on measurement of the source voltage and the DC link voltage. A PWM current control is applied externally with measured and generated source current. A balanced supply voltage at the point of connection is crucial for proper operation of this control. A fully digital controller is implemented in [5]. An attempt has been made to damp the propagation of voltage harmonics in the distribution line. It applies a synchronous rotating frame technique to generate the compensator reference current, and hence the compensator voltage. Sine-PWM technique is used to generate the switching for the voltage source inverter. In [6], the source current reference is generated as an in-phase component of fundamental positive sequence component of the source voltage, calculated by applying synchronous reference frame transformations. However, an analog hysteresis controller is applied to generate switching pulses with the help of a generated source current reference and measured source current to avoid inherent delay of digital current controller. In [7], 4 different control techniques of ShAF are compared at a lower switching frequency of the Voltage Source Converter (VSC). [8] has developed a novel controller based on the Lagrange multiplier optimization technique to generate compensator current reference in DSP. An external hysteresis current controller is implemented to impose the compensator current. In [9], selective harmonic compensation is implemented to generate the reference compensator current. The delay in the measurement and control action, aliasing effect in digitized voltage and current signals due to switching noise are major concerns in any DSP based controller. Synchronous sampling and calculation methods are suggested in [5] to eliminate these effects. Additionally a fast DSP with an Analog to Digital Converter (ADC) of high conversion rate should be chosen for fast control action. Source current reference generation and control instead of the compensator current is suggested in [6] to avoid the spikes in the source current when there is sharp change in the non linear load current. But delay in the control decision and switching can also cause the source current to go out of bands in hysteresis type of current control in spite of direct source current control if a fast DSP and a compact control technique is not chosen.

A compact digital controller to compensate for load current harmonics, load reactive power and load unbalance even under unbalance supply conditions is implemented with a ezDSP F2812 development kit (TMS320F2812 32-bit fixed point processor) for the system shown in Fig. 1. A simple software zero crossing detection based line frequency synchronizing method has been proposed and applied in the control of ShAF. Therefore, a PLL-less control has been achieved which saves the processor time and need of any additional hardware. The DSP implementation of the control has been explained in detail in this paper. The choice of DSP kit is very suitable for the control of ShAF as it contains 16, 12-bit ADC channels, 56 general purpose digital ports of

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which 12 can also act as inbuilt PWM channels, ample on-chip memory as well as external memory and processing speed of 150MHz. The laboratory prototype of the ShAF shown in Fig. 1 was developed. The system parameters, control details and results are presented in the following parts of the paper.

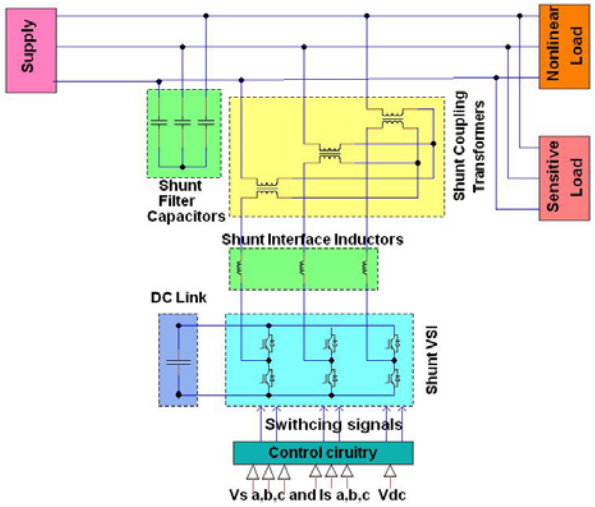

Fig. 1. Power circuit configuration of ShAF with supply load and connecting filters

II. CONTROL AND DSP IMPLEMENTATION

A. ShAF Control

The shunt active filter is controlled as a current controlled voltage source inverter. The measured source current is controlled to stay within the reference band generated with the help of a hysteresis current controller. The control objective can be explained with a block diagram shown in Fig. 2. When applied with a non linear/inductive load, the objective of the shunt converter is to compensate for the load current harmonics, load reactive power and load unbalance such that a unity power factor balanced sinusoidal source current condition is established at the PCC. Therefore, the shunt active filter current is controlled indirectly by controlling the source current to be perfectly sinusoidal and in phase with the source voltage. The fundamental positive sequence in phase and quadrature components of the source voltage (and hence the phase angle) are calculated with (1)-(4).

$$\begin{bmatrix} V_{dp} \\ V_{qp} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \sin(\omega t) & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (1)$$

$$V_{d,q,pos} = \frac{1}{T}\int_{t-T}^{T} V_{dp,qp}\,dt \quad (2)$$

$$\theta = \tan^{-1}\left(\frac{V_{qpos}}{V_{dpos}}\right) \qquad IF\ V_{dpos} > 0 \quad (3)$$

$$\theta = \tan^{-1}\left(\frac{V_{qpos}}{V_{dpos}}\right) + \pi \qquad IF\ V_{dpos} < 0 \quad (4)$$

The phase angle obtained by these components is suitable for calculating the sine template, which is in phase with the positive sequence source voltage. The DC link capacitor is maintained at a reference value. Any variation in the DC link capacitor voltage is the direct measure of the real power requirement of the load. Therefore, the output of the PI controller applied to maintain the DC link voltage constant is the reference magnitude of real power component of the source current as implemented in [4] and [10]. The current magnitude is multiplied by the sine template to generate the reference current. A hysteresis band is constructed by adding and subtracting appropriate offset values to the reference. The measured source current is continuously compared against the hysteresis top and bottom bands to generate the switching pulses. More details on the hysteresis controller can be found in [2]. The compactness of the control and flexibility to work under all load current and source voltage circumstances makes it a very attractive choice to implement in a DSP.

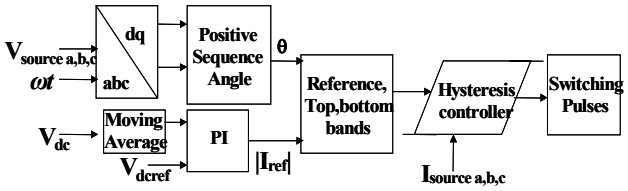

Fig. 2. Control Block of ShAF

B. DSP implementation of control

The control is implemented with a Texas Instrument DSP (TMS320F2812). The power signals to be fed to the ADC have to be conditioned appropriately. The conditioning circuit for phase voltage measurement consists of a resistive attenuating stage, differential amplifier stage, low pass filter stage and a level shifting stage. The source currents are measured with LEM current transducers, passed through differential amplifier, low pass filter and a level shifting circuit. The DC voltage measurement has an appropriate resistive attenuating circuit and a low pass filter. The voltage input to the ADC must be strictly in the scale of 0-3 Volts. Therefore, a transistor based over-voltage protection circuit is built as the last stage of the signal conditioning circuit.

The control software is developed in C using Code Composer Studio environment and loaded on DSP. The Interrupt Service Routine (ISR) where switching decisions are made is operated at around 18 kHz. A frequency locking algorithm is implemented as shown in Fig. 3. The program is started with a 50 Hz approximation of source frequency. The zero crossing of the 'A' phase source voltage at negative to positive half cycle transition is detected with a simple threshold comparison method. A noisy zero crossing is a potential threat for this method of synchronization. To avoid detection of multiple zero crossing, any successive zero

crossing detected is discarded for next 30 samples after the first one is detected. The number of samples for one power cycle is counted. This is compared with a fixed number of samples every time the zero crossing is detected. (360 samples in the present work, considering 18kHz as the sampling frequency). If the grid frequency is higher than 50Hz, a positive difference is calculated. Therefore the speed of the clock synchronized with the ISR and ADC sampling should be increased to synchronize with the grid frequency. Therefore, the clock dividing register value is reduced to increase ISR and ADC sampling frequency. The clock divider is updated in the other way if the grid frequency falls below 50 Hz. The clock divider is adjusted after the detection of every zero crossing, such that the difference between the sample count and the fixed count reduces to zero. Therefore the ISR and ADC sampling frequency will be at or around 18kHz to take into consideration of variation in supply frequency. The register associated with the ISR timer is shadowed in F2812 DSP, which means the register can be updated anywhere in the ISR and can be made effective with different events of the timer (period match and overflow/underflow of counter register).

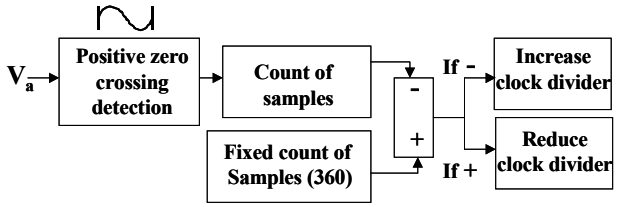

Fig. 3. Frequency locking control block

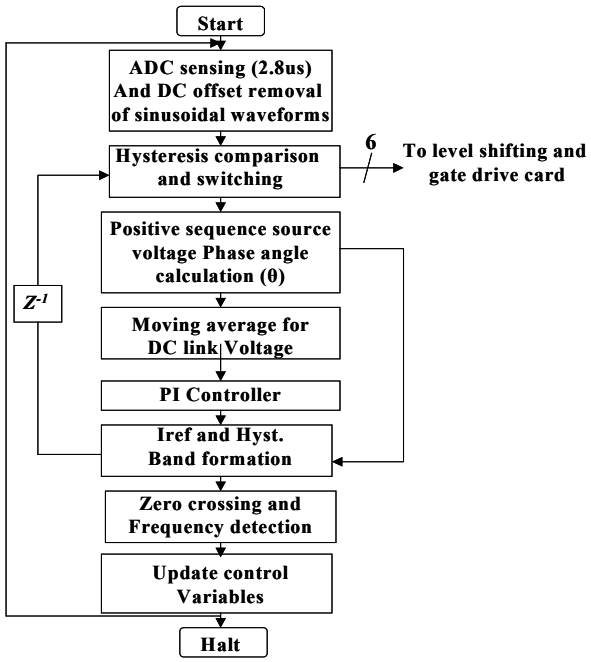

Fig. 4. Flowchart of control

The ADC sampling remains synchronized with the supply frequency since supply frequency is tracked continuously. The inherent delay caused by the ADC sensing and calculations in digital hysteresis controller is of great concern when these types of current controllers are designed. To avoid the delay in switching decisions, the measured source current is compared with the reference value of the current calculated in the previous ISR time. This avoids the delay in switching that can be caused by the calculation time (about 30us). The switching decision is sent to 6 inbuilt General Purpose Input/Output ports (GPIOs). The flow of control followed in Fig. 4 has given satisfactory performance for fully digital control of the ShAF.

The level of the DSP output switching pulses is 0 or 3.3 Volts. The pulses are amplified to a 15 Volts level and a blanking delay of 3 μs is introduced to complementary switching pulses before it is sent to the gate drive circuit of the IGBTs. The protection features such as DC over-voltage and DC over-current are implemented in both hardware and software (Power Drive Protection Interrupt feature of F2812 DSP). The switching pulses are immediately disabled through software during any such abnormal condition.

III. Experimental Setup

The shunt active filter constructed with 6 IGBT switches (150A, 600V) and anti-parallel diodes is connected in a power system as shown in Fig.1. The ShAF is connected to the DC link capacitor (2200μF) maintained at 350V. The load connected is a combination of resistive and inductive elements and a three phase diode bridge rectifier supplying a resistive load. The ShAF is connected to the power system through a 230:130V autotransformer and interfacing inductor (L=1.245mH, R=0.1 Ω). A 20μF capacitor with damping resistor of 4 Ω is connected at the point of common coupling to bypass the switching frequency [11]. This avoids the ShAF switching frequency being fed into the supply. A California Instrument power supply unit has been used and variable loads are used to create the load transients.

IV. Results

The steady state and dynamic performance of the ShAF is presented in this section.

A. Steady state Performance

The frequency locking of generated reference in DSP and voltage input of one of the phases can be seen in Fig. 5. The source frequency is around 50.5 Hz where the reference frequency is generated at 50 Hz, when the program starts. But the generated reference frequency gradually locks to the supply frequency by appropriate adjustment of speed of the ISR clock.

Fig. 6 show the load current as a combination of resistive, inductive and diode bridge rectifier currents. (in Fig. 6 1A peak corresponds to 66mV, peak measured with LEM current transducer LA 205-S). The steady state load current, ShAF current and source current can be seen in Fig. 7 when the ShAF is in action. The THD of the source current measured in the supply unit drops to 4.45% from 15.8% (8%

limit is recommended, by IEEE standard 519-1992). The three phase source current can be seen in Fig. 8. (In Figs. 7,8 and 9 - 1A, peak corresponds to 33mV, peak measured with LEM current transducer LA 205-S)

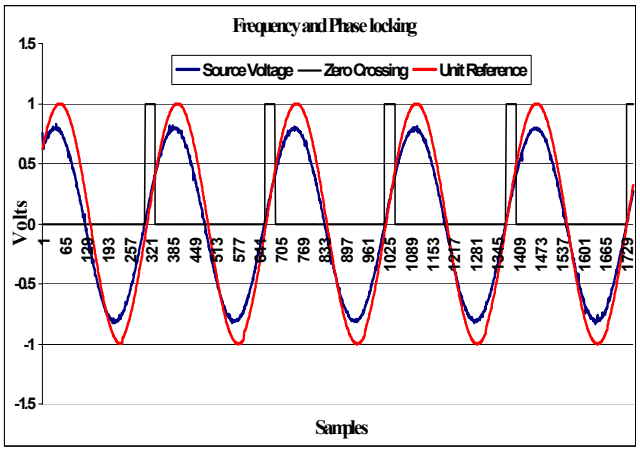

Fig. 5. Frequency locking of reference with grid voltage

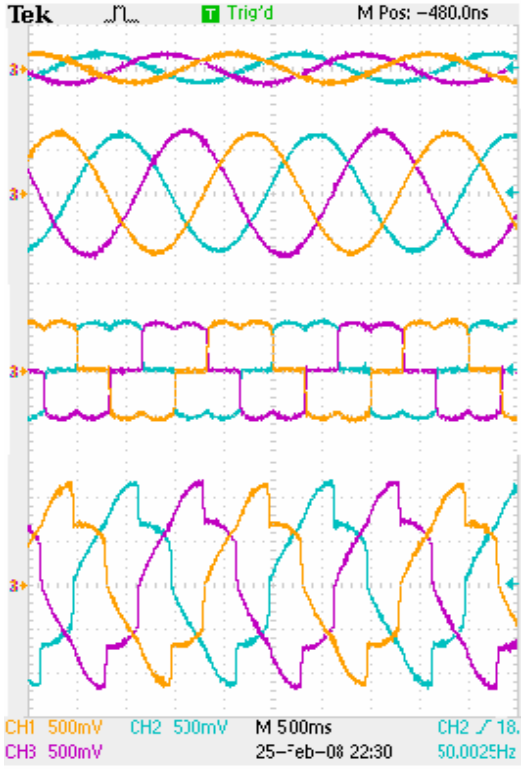

Fig. 6. Resistive, inductive, non-linear and total load current

The compensating action of the ShAF when a load unbalance is created can be seen in Fig. 9. The load and source currents are shown in the Fig.9 respectively.

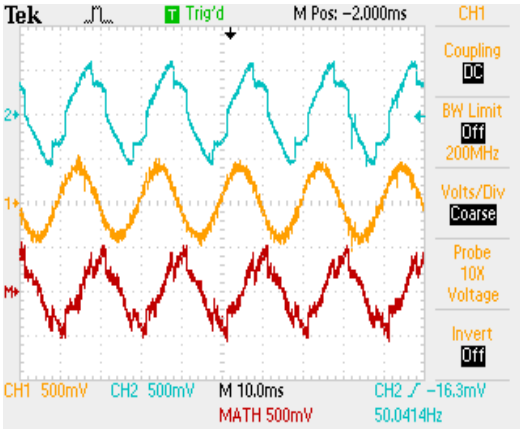

Fig. 7. Load, source and ShAF current in steady state

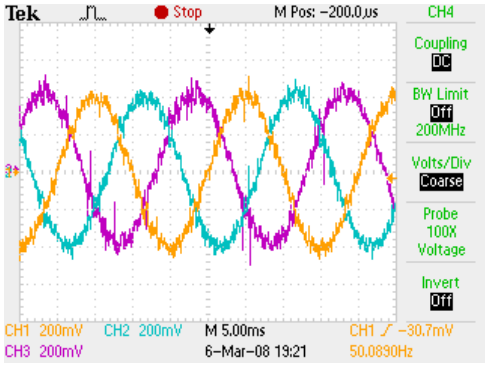

Fig. 8. Three phase source current

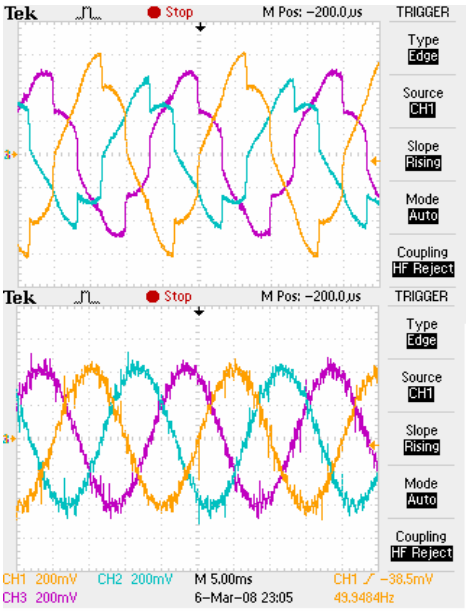

Fig. 9. Load and Source current during load unbalance

B. *Dynamic Performance*

The DC link dynamics during turning nonlinear load on-off can be seen in Fig. 10. The DC link is maintained at 350V by the action of the PI controller. When the nonlinear load is switched off the real power supplied to the load previously is transferred to the DC link capacitor until a new source current reference suitable for the new load condition is calculated. Therefore, the DC link voltage rises above the reference value. Similarly, the DC link voltage drops when a load is suddenly switched on. The controller takes around 6 power cycles to stabilize the DC link voltage. Fig. 10 shows the load current and the DC link voltage during switch on and switch off of a non-linear load.

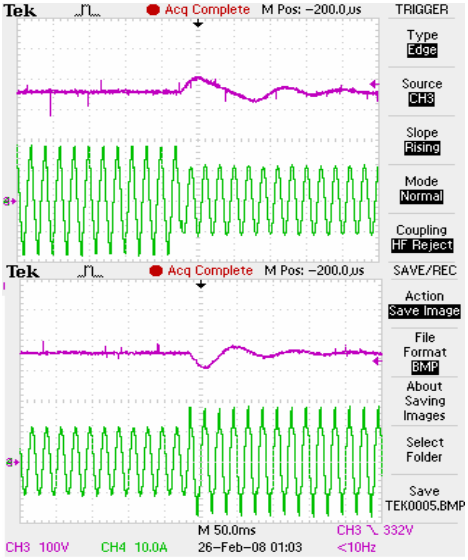

Fig. 10. DC link transients during load on-off

Fig. 11. shows the source voltage (yellow plot) and source current (blue plot) during a load change operation. The non-linear load is suddenly switched on. The magnitude of the source current increases accordingly by control action. But a unity power factor condition is maintained throughout the steady state and transient period as the source current reference is generated by the positive sequence of the source voltage.

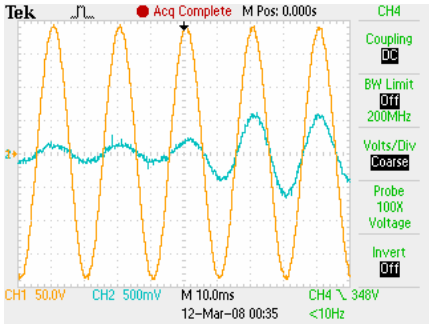

Fig. 11. Source voltage and current

The Harmonics profiles of the load and the source current are given in Fig. 12 and 13 respectively. It can be seen from Fig.13 that the source current harmonics has been reduced to 4.45% from 15.8% by application of the digital ShAF.

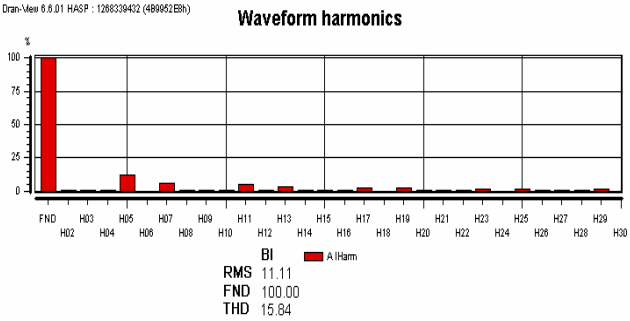

Fig. 12 Harmonics profile of load current

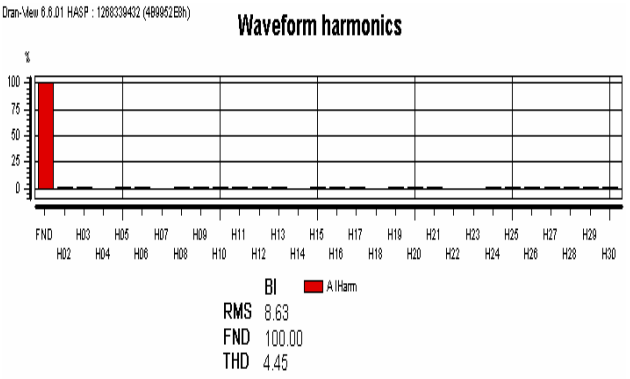

Fig. 13 Harmonics profile of source current

V. CONCLUSIONS

A fully digital controller for ShAF has been implemented with a DSP. A PLL-less grid synchronization method applicable in a digital controller of ShAFs has been proposed and implemented. A compact control algorithm and fast sampling are very important to avoid the current distortion while implementing a digital reference current generator and hysteresis current controller for a ShAF. The THD of the source current is improved from 15.8% to 4.45% (8% limit is recommended by IEEE standard 519-1992) with the implemented digital controller. The performance of the DSP controller has been found out to be very satisfactory.

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