



2003

A Simulation Model to Characterize Photolithography Process of a Semiconductor Wafer Fabrication

Amr Arisha

Dublin Institute of Technology, amr.arisha@dit.ie

Paul Young

Dublin City University

Mohie El Baradie

Dublin City University

Follow this and additional works at: <http://arrow.dit.ie/buschmarcon>



Part of the [Other Operations Research, Systems Engineering and Industrial Engineering Commons](#)

Recommended Citation

Arisha, A., Young, P., El Baradie, M.: A Simulation Model to Characterize Photolithography Process of a Semiconductor Wafer Fabrication. Nineteenth International Manufacturing Conference (IMC21), Ireland.

This Conference Paper is brought to you for free and open access by the School of Marketing at ARROW@DIT. It has been accepted for inclusion in Conference papers by an authorized administrator of ARROW@DIT.

For more information, please contact yvonne.desmond@dit.ie, arrow.admin@dit.ie, brian.widdis@dit.ie.



This work is licensed under a [Creative Commons Attribution-NonCommercial-Share Alike 3.0 License](#)



A SIMULATION MODEL TO CHARACTERIZE PHOTOLITHOGRAPHY PROCESS OF A SEMICONDUCTOR WAFER FABRICATION

A. Arisha¹, P. Young¹, and M. El Baradie¹

1. School of Mechanical and Manufacturing Engineering, Dublin City University, Dublin9, Ireland; email: amr2000@gmx.net

ABSTRACT

The pressures on semiconductor manufacturers due to cost considerations, rapid growth of process technology, quality constraints, feature size reduction, and increasingly complex devices are increasing requiring ever higher efficiency from the manufacturing facilities. The complexity of manufacturing high capacity semiconductor devices means that it is impossible to analyze the process control parameters and the production configurations using traditional analytical models. There is, therefore, an increasing need for effective models of each manufacturing process, characterising and analyzing the process in detail, allowing the effect of changes in the production environment on the process to be predicted. The photolithography process is one of the most complex processes in a semiconductor manufacturing environment. Using state-of-the-art computer simulation and a structured modelling methodology a generic model of photolithography flexible manufacturing cells has been developed and used to mimic actual performance of the tools. Comparison of the output from the model with data from the plant showed the quality of the model. This paper discusses the technique used to develop the simulation model to characterize the photolithography process tools. Details on the structured modelling approach taken to develop reusable simulation models have also been presented. Conclusions and recommendations to maximize the process performance and reduce risk have been included.

Keywords: Photolithography Process, Simulation, Semiconductor manufacturing

1 INTRODUCTION

Semiconductor manufacturing is one of the most complicated manufacturing systems in terms of technology and procedure. Traditional industrial engineering analysis techniques through mathematical models or even deterministic models to study manufacturing areas are simply not adequate to analyze these complex manufacturing environments. These have to be modelled and optimized by means of powerful techniques such as simulation and system analysis approaches (e.g. IDEF0, design of experiment), in order to properly model the dynamics as well as variability of the system. The photolithography process is considered the most complex process in the wafer fabrication due to complex technology, critical dimensions, and re-entrant flow [1]. Much research has been carried out into various aspects of the electronic manufacturing in general [2] and semiconductor in particular [3]. Some research has investigated in detail specific process parameters such as cycle times [4]. From the literature as well as industrial sources, there is no overall methodology exists through which a systems approach can be employed. Few researches have been published on photolithography process in semiconductor manufacturing [5]. This paper

presents a generic systematic methodology for optimizing photolithography process parameters. The proposed methodology integrates three techniques to generate efficient model for analysis, control, and optimization of photolithography tools.

2 PHOTOLITHOGRAPHY PROCESS

The wafer fabrication processes can be divided into six basic processes as shown in figure 1.

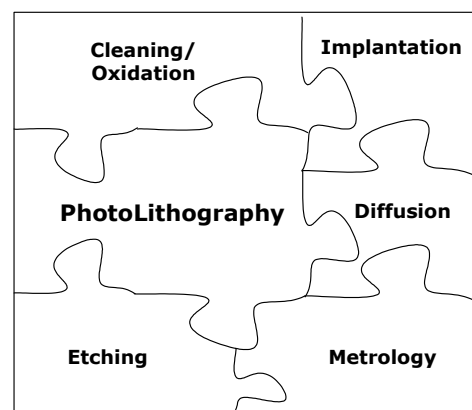


Figure 2. Wafer fabrication jigsaw

Photolithography lays down patterns on layers, allowing other processes (e.g. oxidation, etching, ion implantation) to produce the required circuit devices and interconnections. Most

photolithography processes have a similar process flow within limited variations. The process has mainly three sets of operations includes “Spin/Coat” operations, “Align/Expose” operations, and “Develop” operations as illustrated in figure 2.

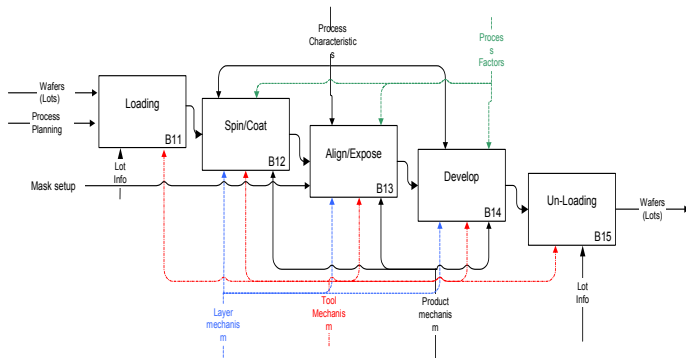


Figure 2. Photolithography process steps

3 PHOTOLITHOGRAPHY MODEL

The aim of the photolithography process tool model is to offer the manufacturer a systematic methodology to understand the behaviour of the process better and achieve optimal operating conditions. The model presents a comprehensive integration of three analytical techniques, IDEF, simulation, and design of experiments, figure 3, in order to;

1. Build an effective hybrid model to characterise photolithography process;
2. Determine the significance of the impact of process control parameters;
3. Enhance the process performance by determining the optimal combinations of process parameters;
4. Provide a state-of-the-art simulation model to economically examine the process performance under different production scenarios.

3.1 Process Constraints

The main constraints imposed on the model are two main groups; constraints due to the technology complexity, and constraints due to production. The first group includes operation sequence, setup times, processing times, and metrology. While the other group involves the lot integrity, re-entrant flow, product/layer sequence, storage (buffers), and preventive and unscheduled maintenance.

3.2 Process Parameters

In most of the cases, the photolithography process can run uninterrupted after a lot is loaded on the manufacturing cell. In this study, the effect of some key process control parameters (e.g. wafers start

(WS), number of products/product-mix (PM), dispatching rules (product sequence), and stepper buffer size (BS)) on the performance of photolithography flexible manufacturing cell were examined. The performance measures of interest were makespan, cycle time, and utilization.

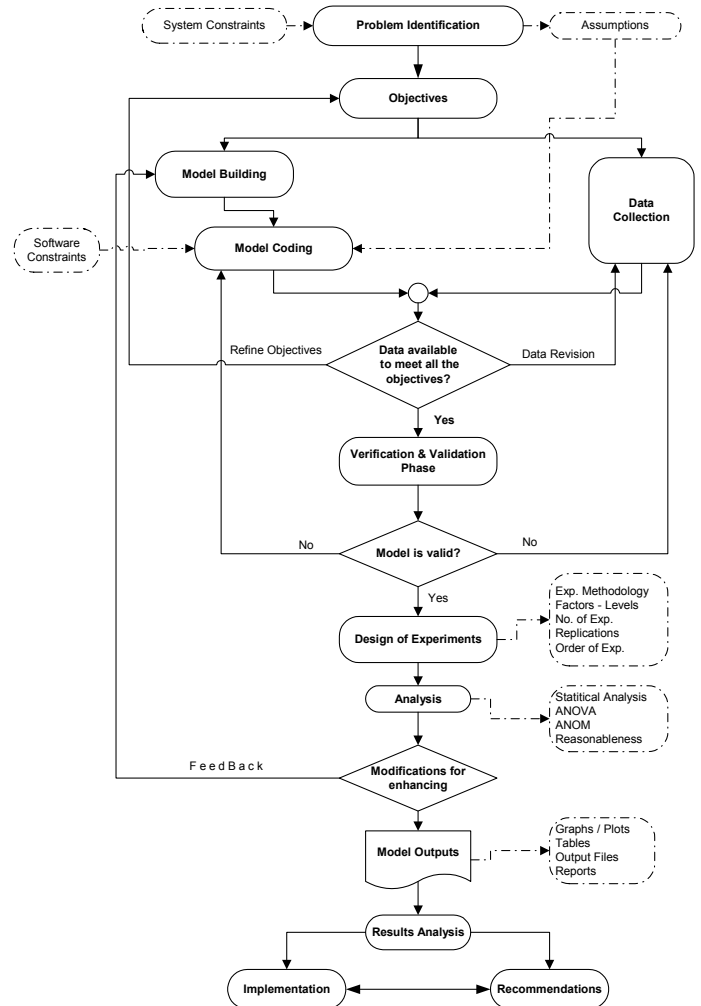


Figure 3. Methodology Steps

3.3 IDEF0 Model

IDEF0 is one of the most effective tools to model complex industrial systems. Process modelling starts with a basic function and then breaks it down into sub-levels. The basic element is a function block, which can be decomposed into more detailed sub-function blocks further down the hierarchy. Further information about IDEF0 can be found in [6].

Every set of operations of the photolithography tool modelled in detail. Figure 4 shows detailed modelling of the exposure operation. The after operations were also broken down this way.

5 SIMULATION EXPERIMENTS

Experimental design framework was adopted to provide a convenient procedure for conducting the main simulation runs [9]. This helps in determining suitable factor (level) combinations to give near-optimal performance measure estimates.

Based on the analysis of means (ANOM), the near optimum level for each factor can easily be identified as the level that results the minimum average throughput time (TPT), figure 6. The analysis of variance (ANOVA) (Table 1) shows the significance of individual factors by establishing the relative magnitude of the effect of each factor on the objective function.

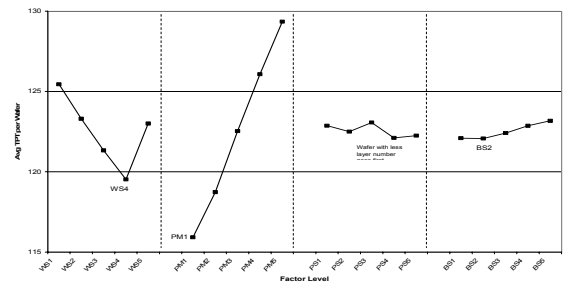


Figure 6. ANOM of factors main effect

Table 1. ANOVA Matrix

Factor	(DOF)	(SSB)	(SSB/DOF)	F
WS	4	0.499298	0.124825	16.126
PM	4	2.946854	0.736714	95.1765
PS	4	0.023777*	0.005944	
BS	4	0.023888*	0.005972	
Error	8	0.076183*	0.009523	
Total	24	3.57		
(Error)	(16)	(0.123848)	(0.0077405)	

* Indicates the sum of squares added together to estimate the pooled error sum of squares, indicated by parentheses. The F ratio is calculated using the pooled error mean square.

A number of simulation sensitivity analyses were performed, including experiments to analyze the variation in cycle times through each of the steps detect the process bottleneck(s). The results are shown in figure 7.

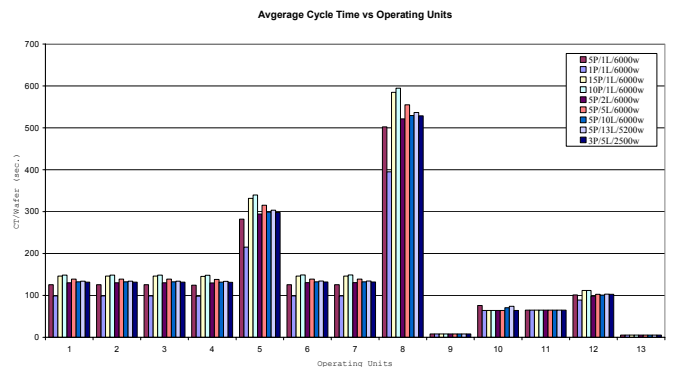


Figure 7. Variations in photolithography steps average cycle times

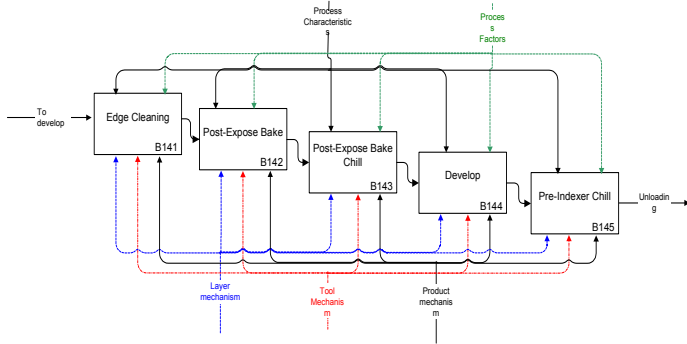


Figure 4. Exposure operations in detail

4 SIMULATION MODEL

Building the simulation model started with the assumptions and reviewing the constraints with the manufacturing team [7]. The simulation model aims to provide a reusable generic model of the photolithography process tools.

4.1 Simulation Output

A host of simulation output measures can be obtained from the model which may be useful for characterisation. Of these the following were considered the most relevant:

- Process equipment throughput time
- Photolithography step throughput time
- Work In Process (WIP) inventory level
- Cycle Time per wafer/lot (CT)
- Equipment utilization

4.2 Model Verification and Validation

The strength of decisions made based on the simulation model is a direct function of the validity of this data [8], hence the need for efficient and objective methods to verify and validate the model. The verification and validation of the model took place as a continuous process [7]. The simulation model was verified using three approaches and found to be effective in comparison to an existing model, figure 5.

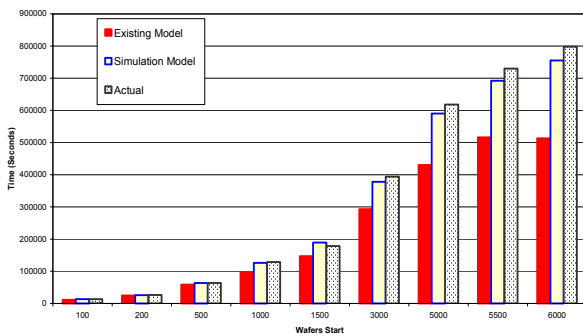


Figure 5. Comparison between simulation output, actual data, and deterministic models

6 RESULTS DISCUSSION

Based on the ANOM plot in figure 6 and ANOVA detailed in table 1, the process control parameters (i.e., the number of wafers start and product-mix) have a statistically significant impact on the total throughput time and the TPT per wafer. The results suggest that experimentation should focus attention on the alternatives available for the product-mix and wafers start and only then the other parameters for improving the global performance. The sensitivity study of the variation in cycle times through each step in the photolithography process helps to identify the bottleneck steps in the manufacturing cell. Generally speaking, the quality of any simulation approach is measured in at least two dimensions: (1) how close the output comes to the real system if it can be measured; and (2) how much computer time is required to solve problems of a given size [1]. The simulation model has shown reasonable results and better understanding of the cell behaviour under various operating conditions. The quality of the output has been verified with actual floor data of similar conditions. The computer time required to run the simulation model for one experiment was economic, less than three minutes on Pentium IV processor.

7 CONCLUSIONS

The paper presents an approach including three effective techniques namely; IDEF0, simulation, and experimental design. This systematic approach has been successfully developed to characterize the photolithography process and to optimize selected process control parameters. The effective use of experimental design procedure in optimizing the process control parameters has a significant impact on decision-making within complex flexible manufacturing environments. The proposed design of experiments can be used to optimize the level for different process control parameters helping manufacturing staff to focus on setting priorities among the process parameters.

The development of a reusable generic simulation model to characterize the photolithography process in wafer fabrication has provided a robust tool to examine the impact of various production changes on the photolithography process. The model has been successfully verified and validated and the results used directly by production staff. The model has also reduced the turnaround time in evaluating the impact of policy decisions on the manufacturing performance.

ACKNOWLEDGEMENTS

This research was supported by Intel-Ireland. We would like to thank Mr. Ger Ryan, and Mr. Michael O'Dwyer (Intel) for their extensive help during research time.

REFERENCES

- [1] A. Arisha, *Intelligent shop scheduling for semiconductor manufacturing*, PhD thesis submitted 2003, Dublin City University, Ireland, (2003).
- [2] A. Doniavi, *Computer aided systems engineering approach to electronic manufacturing*, PhD thesis, University of Bath, UK, (1999).
- [3] R. Uzsoy, Chung-Yee Lee, and L. Martin-Vega, *A review of production planning and scheduling models in the semiconductor manufacturing, Part I*, IIE transaction on scheduling and logistics, Vol. 26, pp 44 – 55, (1994).
- [4] Akcali, E., Nemoto, K., and Uzsoy, R., *Quantifying the Benefits of Cycle-Time Reduction in Semiconductor Wafer Fabrication*, IEEE Transactions on Electronics Packaging Manufacturing, Vol. 23, pp 39 – 47, (2000).
- [5] D. Williams, and D. Favero, *Dynamic Deployment Modelling Tool for Photolithography WIP Management*, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pp 55 – 58, (2002).
- [6] United States Air Force, *Integrated Computer Aided Manufacturing (ICAM)*, Architecture Pt II, Vol. IV, Function Modelling Manual (IDEF0). Air Force Materials Laboratory, Wright-Paterson AFB, Ohio, 45433, AFWAL-TR-81-4023, June (1981).
- [7] J. Banks, *Introduction to Simulation*, WSC 2000, pp 9 – 16, (2000).
- [8] N. Nayani, and M. Mollaghasemi, *Validation and verification of the simulation model of a photolithography process in semiconductor manufacturing*, WSC 1998, pp 1017-1022, (1998).
- [9] M. S. Phadke, *Quality Engineering Using Robust Design*, Prentice-Hall International, Englewood Cliffs, NJ, (1989).