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Sequence analysis based DSP controller for Dynamic Voltage Restorer (DVR)

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***Abstract*—The paper examines the behaviour of a Dynamic Voltage Restorer (DVR) under balanced/unbalanced supply voltage sag condition, and restricted DVR injection capability (e.g. limited to 50% of the supply voltage injection). Sequence components of the supply voltage are extracted to generate the reference injected voltage for the DVR. The control determines the maximum possible positive sequence injection within the capacity of the compensator to achieve balanced voltage conditions at the load terminals. The control is verified through simulation and experimentation. The control algorithm has been implemented in a TI320F2812 fixed point DSP and the effectiveness of the controller is verified in a three-phase, 10kVA DVR laboratory prototype. In a three-phase, 240 V system, balanced sag and sag with magnitude and phase unbalance have been created, which is successfully compensated by the DVR with the proposed controller.**

I. INTRODUCTION

The Dynamic voltage restorer (DVR) offers sensitive voltage customers dynamic protection against system voltage disturbances originating from the incoming transmission/distribution system. DVRs could also form the series compensator part of Unified Power Quality Conditioners (UPQC) to serve the above purpose [1]. Typically a DVR/UPQC is installed at the service entry point of sensitive voltage zone to compensate for voltage disturbances like sag/swell or unbalance, such that the voltage across a critical load terminal is perfectly regulated [3]-[6]. In this paper a sequence based compensation strategy has been developed to compensate balanced or unbalanced incoming voltage to regulate the load voltage. The advantage of the scheme is that under all conditions of unbalance, the DVR controller is able to compensate the unbalance, even if the voltage capability of the DVR is limited by its rating, which may be decided by some other governing factors such as cost of the equipment, and/or over all UPQC rating.

Fig. 1 shows the schematic diagram of a series compensated system for load voltage regulation. The DVR system consists of a three-phase voltage source converter (VSC), low pass filter and injection transformer. The DVR is designed such that the maximum balanced voltage sag compensation is restricted to 50% of the supply voltage. The DVR is controlled from a TMS320F2812 TI fixed point DSP controller. The detailed parameters of the test system are described in Section III.

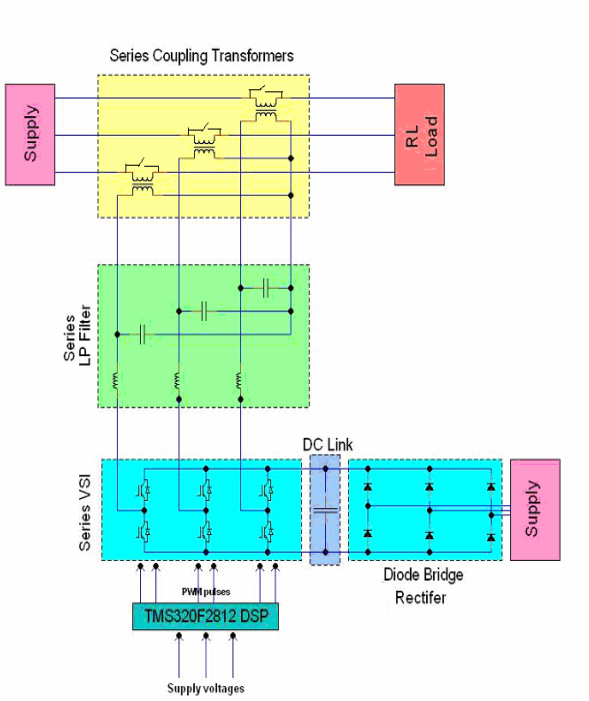

Fig. 1. Power circuit of DVR

II. WORKING PRINCIPLE AND CONTROL OF DVR

A. *Working Principle of DVR*

A DVR maintains the load voltage at a predetermined level during any source voltage abnormal conditions such as voltage sag/swell or distortion. The working principle of the DVR can be explained with the help of Fig. 2. Three phase voltage phasors Va1,Vb1 and Vc1 are balanced with 100% magnitude under normal operating condition. A fault in the upstream of the PCC

can cause a balanced or unbalanced voltage disturbance at the PCC depending on the type of the fault.

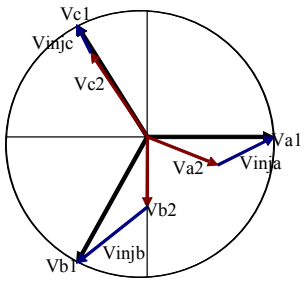

Fig.2. Voltage Phasor

During an unbalanced fault situation, the phase voltage vectors may be altered to Va2, Vb2 and Vc2. The situation here is that of a typical line to line fault which does not involve grounding. The DVR can inject appropriate voltages Vinja, Vinjb and Vinjc in order to build a balanced three phase system of voltage vectors Different types of voltage compensation strategy are discussed [2]-[8]. In [7] an attempt has been made to reduce the system losses by keeping the exchange of real power between the DC link and supply to a minimum. This is achieved by injecting voltages in quadrature to the supply current. This type of DVR does not need any DC link support since no real power is involved in voltage injection. But during deeper sags, a high rating of inverter is necessary for compensatory action. The sequence component based analysis carried out in [8] suggests that the most economical voltage injection can be achieved by re-aligning the voltage vectors according to the positive sequence component.

B. Sequence Component Control of DVR

A sequence analysis based control strategy is adopted in this paper. The phase voltages are converted to balanced system of positive (V_1), negative (V_2), and zero(V_0) sequence components. The DVR control aims to maintain the positive sequence component at a predetermined value and to reduce the negative sequence and zero sequence components to zero. The zero sequence component in the three phase three wire system considered here is zero. Therefore, the injected voltage *Vinj* of a particular phase can be written as the vector sum of reference voltage (*Vref*), positive (*V1*) and negative(*V2*) sequence voltages, as given in (1).

$$\overrightarrow{Vinj} = \overrightarrow{Vref} - \overrightarrow{V_1} - \overrightarrow{V_2} \qquad (1)$$

The *Vinj* adds to the source voltage to regulate the load voltage at the desired level. The voltage that can be injected by the DVR in order to establish a balanced three-phase system is determined by the rating of its inverter. If the desired magnitude of *Vinj* is beyond the capacity of the inverter of the DVR like one of the cases considered in this paper, it has to be limited to the maximum voltage capacity of the inverter. In case of a balanced voltage sag/swell, the negative sequence component will be zero. Therefore, only positive sequence in-phase injection of the voltage up to the maximum capacity of the DVR will maintain the balance in the load voltage with maximum possible amplitude (*Vmax*). But under severe voltage unbalance conditions, limiting the magnitude of the calculated *Vinj* will not ensure a balanced voltage condition at the load terminals. Therefore, it is necessary to determine the maximum amplitude and angle of injection of the voltage that can be injected in order to establish a system of balanced three phase load voltages with maximum possible amplitude. Determination of the appropriate *Vinj,* under restricted inverter rating is the key research question of this paper.

The voltage to be injected which is the combination of positive and negative sequence is calculated. The phase which requires maximum injection is selected and following three possible cases of *Vinj* are defined in the control.

(1) *Vinj* <= *Vmax*

When calculated voltage magnitude is within the capability of the compensator, no further calculation is required. Thus injected voltage is the calculated voltage.

(2) *Vinj*>*Vmax* and *V2*>*Vmax*

When calculated voltage magnitude is higher than the maximum possible voltage and negative sequence magnitude is higher than the maximum possible voltage, maximum possible negative sequence voltage is injected.

(3) *Vinj*>*Vmax* and *V2*<*Vmax*

When calculated voltage magnitude is greater than *Vmax* but negative sequence magnitude is lower than *Vmax*, appropriate positive sequence magnitude has to be selected in order to keep the injected voltage magnitude equal to the maximum possible magnitude. The selection of positive sequence component is explained with the help of a phasor diagram shown in Fig. 3. *OA* is the voltage of one of the phases which requires maximum voltage injection during the fault. *OG* is the reference voltage set along the positive sequence component of that phase. The voltage *AG* has to be injected in order to establish the reference voltage in this phase. *AG* is the combination of positive (*EG*) and negative sequence (*AE*) components. In case the compensator is unable to inject *AG* and *AF* (*Vmax*) is the maximum possible injection to establish a balanced voltage condition, the positive sequence magnitude has to be reduced to *EF*. The magnitude *EF* that can be injected in this situation can be calculated from (2)-(5):

$$|GD| = |AG| * \sin\beta \qquad (2)$$

$$|AC| = \sqrt{|V\max|^2 - |GD|^2} \quad (3)$$

$$|AB| = \sqrt{|AE|^2 - |GD|^2} \quad (4)$$

$$|BC| = |EF| = |AC| - |AB| \quad (5)$$

Therefore injected voltage is restricted to combination of negative sequence component and reduced positive sequence component in all phases in order to stay within the limit of the compensator.

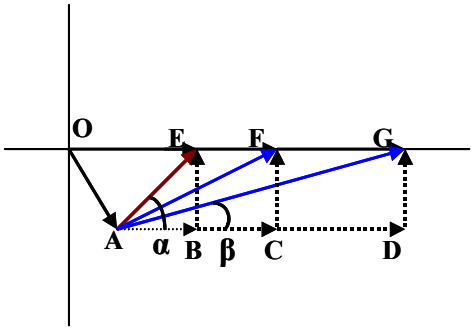

Fig. 3. Injected voltage vector calculation

III. Simulation and Experimental Setup

The power circuit of the DVR is shown in Fig. 1. It consists of a three-phase full bridge voltage source inverter built with IGBT switches. It is connected in series with three-phase 240 V power system with 4kVA (130V:115V) single-phase transformers. A series low pass LC (1.245mH, 10μF per phase) filter is connected to remove the switching noise. The inverter has a 2200μF DC link capacitor (operating at 230 V, and powered by a diode bridge rectifier). A 2 kVA R-L load is connected for all tests. The voltage sag profiles are created with the help of California Instrument AC source unit.

A detail simulation model of the system is developed in SimPowerSystem Toolbox of MATLAB/Simulink. The inverter, diode bridge rectifier, DC link, coupling transformers and low-pass filters are represented as in the actual experimental setup in the discrete model. Sine-PWM switching pulses are supplied to the inverter at 10kHz frequency.

The control developed in Section II is implemented with a control optimised fixed-point TI DSP (TMS320F2812). A feed-forward control loop measures the source voltage continuously and it is compared with the reference voltage to be maintained at the load. The appropriate voltage to be injected is calculated and switching information is sent to the IGBT switches. The in-built PWM ports of the DSP provide switching pulses at 10 kHz frequency. The control block is given in Fig. 4.

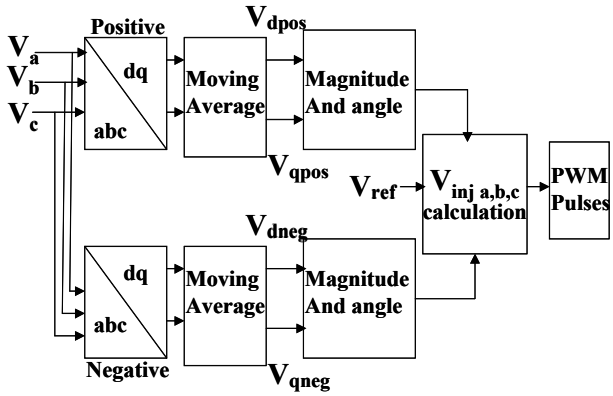

Fig. 4. Control Block of DVR

Three phase voltages are sensed and converted to positive and negative sequence in-phase and quadrature components as shown in (6) –(8). The magnitude and phase angle of the positive and negative sequence components are calculated. The appropriate voltage to be injected is calculated as explained in section II.

$$\begin{bmatrix} V_{dp} \\ V_{qp} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} sin(\omega t) & sin(\omega t - 2\pi/3) & sin(\omega t + 2\pi/3) \\ cos(\omega t) & cos(\omega t - 2\pi/3) & cos(\omega t + 2\pi/3) \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} V_{dn} \\ V_{qn} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} sin(\omega t) & sin(\omega t + 2\pi/3) & sin(\omega t - 2\pi/3) \\ cos(\omega t) & cos(\omega t + 2\pi/3) & cos(\omega t - 2\pi/3) \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (7)$$

The positive and negative sequence components which are transformed to DC in (6) and (7) are extracted with the help of a moving average filter (acts as a low pass filter) over a period of one power frequency cycle as shown in (8).

$$V_{d,q,pos,neg} = \frac{1}{T}\int_{t-T}^{T} V_{dp,qp,dn,qn}\,dt \quad (8)$$

$$|V_{pos,neg}| = \sqrt{V_{dpos,neg}^{\ 2} + V_{qpos,neg}^{\ 2}} \quad (9)$$

$$\angle_{pos,neg} = tan^{-1}\left(\frac{V_{qpos,neg}}{V_{dpos,neg}}\right) \quad (10)$$

$$V_{inj} = |V_{ref} - V_{pos}|\angle_{pos} - |V_{neg}|\angle_{neg} \quad (11)$$

The slight variation in the system frequency is taken care by a software phase locking, in which the interrupt generating register period is adjusted according to the zero crossing of the system voltage detected in the software.

IV. RESULTS

A. Simulation Results

A 30% balanced voltage sag is created at 0.1 sec and cleared at 0.3 sec. 140V rms is the reference voltage at the load terminals. The load voltage is maintained at 140V during the sag period with the help of DVR. The source voltage, load voltage and the injected voltage are shown in Fig. 5.

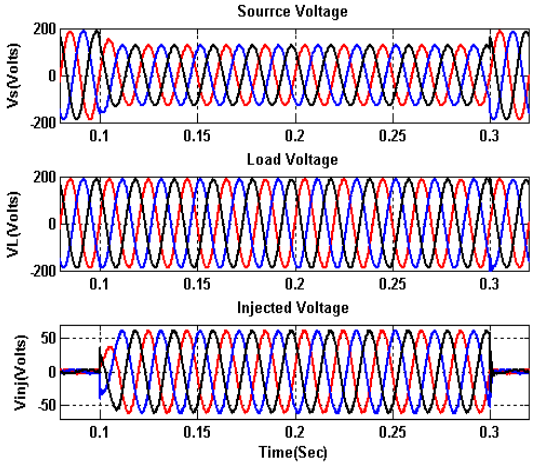

Fig. 5. Source, load and injected voltage during a balanced sag (simulation)

Fig. 6 shows the phase A source, load and the injected voltages. The injected voltage is in-phase with the source voltage. The DC link is supported by a diode bridge rectifier to carry out appropriate in-phase injection.

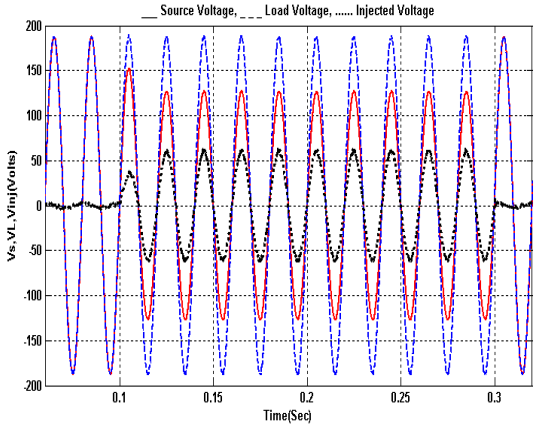

Fig.6. A phase source, load and injected voltage (simulation)

Fig. 7 shows the source, load and injected voltage when a unbalanced voltage sag is created. ($V_a = 90\sqrt{2}\angle 0^o, V_b = 90\sqrt{2}\angle -90^o, V_c = 127.3\sqrt{2}\angle 135^o$).

The appropriate voltages in different phases are injected to balance the system and mitigate the voltage sag.

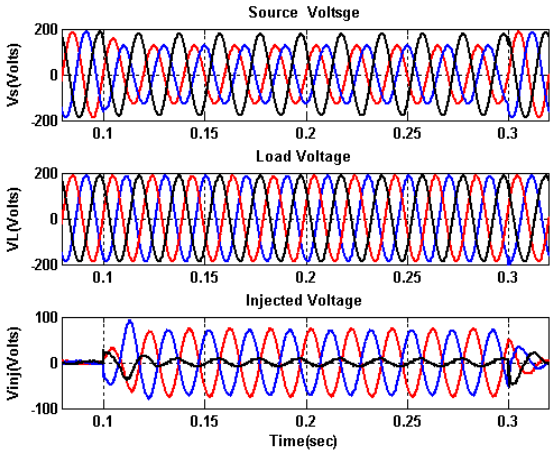

Fig.7. Source, load and injected voltage during a unbalanced sag (simulation)

B. Experimental Results

The source voltage is reduced to 90V rms from 140V rms to create a balanced sag condition. 50 V rms is injected from the DVR to maintain the load voltage constant. The source, injected and load voltages can be seen in Fig. 8.

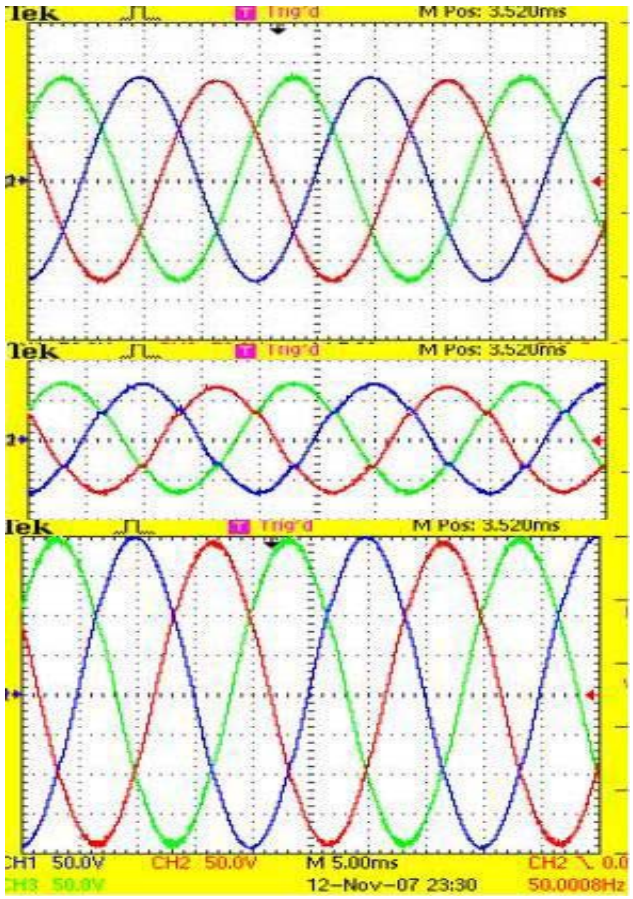

Fig. 8. Source, injected and load voltage during a balanced sag (experiment)

Fig. 9 shows the load voltage transients during voltage sag. It is compensated within 3 power cycles which can be observed in Fig. 9.

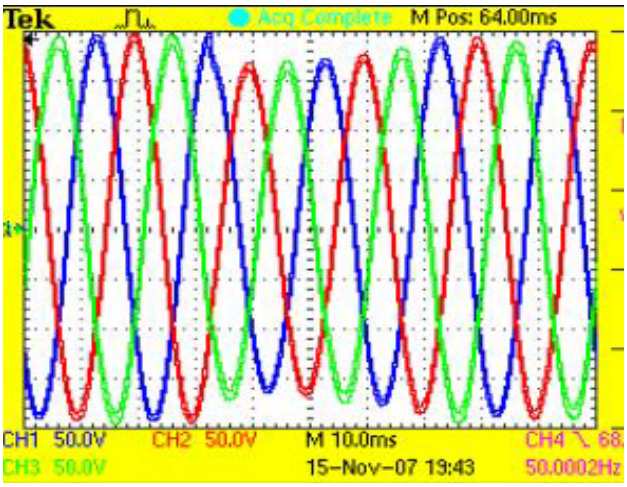

Fig. 9. Load voltage transients during voltage sag (experiment)

The source, injected and load voltage during an unbalanced sag is shown in Fig.10. The a,b,c voltages are as given above for the simulation.

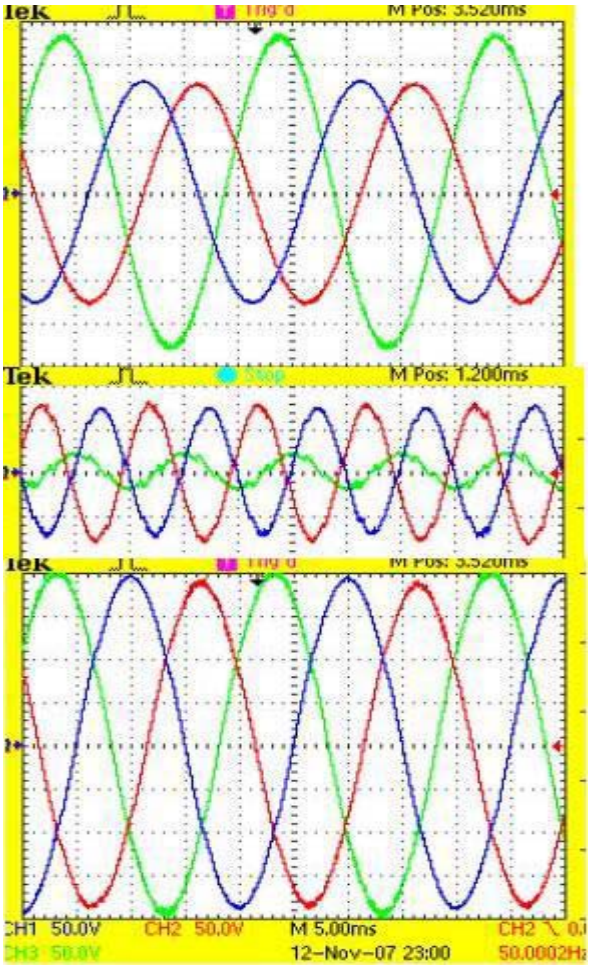

Fig . 10. Source, injected and load voltage during a unbalanced sag (experiment)

The results shown in Fig. 11 represent the compensator action under a limited injection condition. The unbalance voltage profile created is

$$V_a = 45\sqrt{2}\angle 0^o, V_b = 45\sqrt{2}\angle -90^o, V_c = 63\sqrt{2}\angle 135^o$$

In order to verify the controller capability, the maximum compensator voltage is limited to 50% of the nominal voltage (70V rms). Therefore It is not in the capacity of the compensator to provide 100% magnitude compensation. Since negative sequence magnitude is lower than the maximum limit of the voltage, perfect voltage balance at the load terminals is restored. Fig 11 shows the source, injected and load voltages.

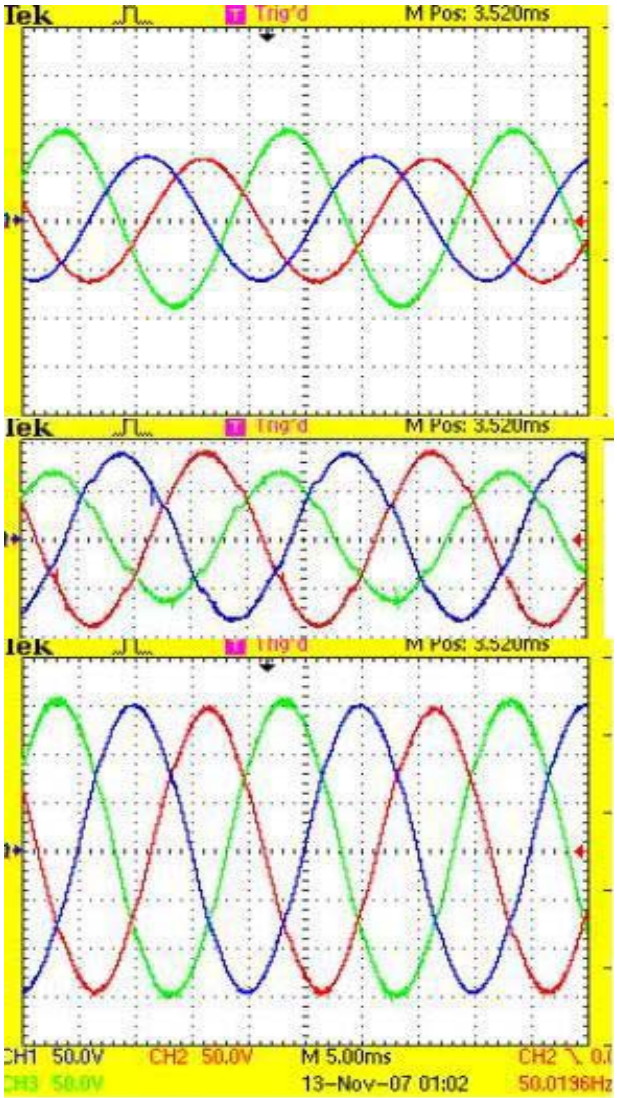

Fig. 11. Source, injected and load voltage during a unbalanced sag with limited injection (experiment)

V. CONCLUSIONS

A sequence component based controller has been developed for a DVR. The performance of the controller is verified both in simulation and experimentation. The controller is simple but elegant to implement with a DSP. Experimental results are found to be satisfactory to validate the proposed control algorithm. The advantage of the scheme is that under all conditions of unbalance/phase jump, the DVR controller is able to compensate the unbalance, even if the voltage capability of the DVR is limited by its rating, which may be determined by some other governing factors such as cost of the equipment.

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